Amendments to the Specification:

Please replace paragraph [0031] with the following replacement paragraph.

[0031] FIG. 2 shows a timing diagram showing relationships between various signals in the circuit of FIG. 1: external synchronization signal 174, system clock signal 170, gauge signal (pulse) G1 196, VCO output clock signal 166 and gauge signal (pulse) G2 198. The timing diagrams are exemplary only and other variations are possible, for example, external synchronization signal 174 is shown as a negative going pulse that is active on its trailing edge but it could, in other embodiments, be a positive going pulse or another form. FIG. 2 shows the relationship between the trailing (rising) edge 201 of external synchronization signal 174 to the leading (rising) edge 202 of gauge signal G2 198 and the first synchronized edge 203 of VCO output signal 166. In the example[[,]] timing diagram of FIG. 2, each counter is set to count 13 half-cycles of clock signal for the pulse width since 13 half-cycles facilitates diagramming, but practical embodiments will typically use pulses having a duration of many more than 13 half cycles of clock signal. FIG. 2 also shows the relationships between the trailing (rising) edge 201 of external synchronization signal 174, the next rising edge 213 of the reference clock signal 170, and the leading edge 212 of gauge signal G1 196.